layer structure on a semiconductor substrate comprising providing a semiconductor substrate, depositing a first layer having a series of lattice-mismatched semiconductor layers on the substrate, annealing the layer at a temperature greater than 100°C above the deposition temperature, depositing a second layer on the first layer with a greater lattice mismatch to the substrate than the first layer, and annealing the second layer at a temperature greater than 100°C above the deposition temperature of the second layer.

The proposed combination of references by the Examiner simply does not meet the limitations of the independent claims. Furthermore, the references are not properly combinable.

It is acknowledged that the teachings of Jewell '864 show a lattice-mismatched layer on a substrate with a subsequent lattice-mismatched layer. Such a step-graded or graded layer system was well known decades before Jewell '864. However, the intent of the present invention is to improve upon graded layer systems deposited under potentially optimal conditions that lead, inherently, to inferior material due to other constraints.

For example, the invention refers to the situation in which it is optimal to deposit graded layers at the highest temperature possible, yet other issues in CVD reactors result in inferior material quality. In this case, by annealing layers that have been deposited with increments in lattice-mismatch, one can achieve the benefit of high dislocation velocity without the deleterious reactor problems that occur with continuous high temperature growth.

Therefore, it is the combination of the short, high temperature anneals with the graded layer structure that allows material to be grown of unprecedented quality. With regards to the annealing procedure, the Examiner has referenced Bensahel '750 in column 1, line 64, to indicate that combining annealing with step-graded structures would be obvious. This

reference in Bensahel '750 is in fact from the work of G. Kissinger et al., APL 66, 2083 (1995).

The invention as claimed would not be obvious based on known graded work (like Jewell) and Kissinger et al.. Since a renewed interest in relaxed graded layers in 1991, all high quality graded layers reported were achieved by depositing the graded layers at high temperatures. With the exception of Kissinger et al., no reference is found to any graded layers deposited with annealing to improve final threading dislocation density, even after publication in 1995. One reason is that Kissinger et al. emphasizes that very long anneal times on the order of an hour or fraction of an hour are necessary to achieve low threading dislocation densities.

An immediate conclusion is that such a technique is not useful, since production times would be increased from minutes to fractions of a day per wafer, and growth time is directly related to final wafer cost. Thus, such a procedure is impractical since wafers cannot be created economically. Kissinger et al. inherently suggests that the results require such long anneal times, as indicated on page 2084 "..although any other growth technique should be usable that permits the *in situ* annealing of high temperatures for extended periods of time".

Besides being impractical and not motivating one skilled in the art to pursue such a combination for long or short anneal times, the Kissinger method was used by the Applicant to try and reduce threading dislocation density. Applicant saw absolutely no decrease in threading dislocation density for extremely long anneal times in the fashion practiced by Kissinger et al. Applicant contends that the data from the Kissinger et al. paper is suspect based on the dislocation velocities that can be extracted from the paper. Based on the

Kissinger et al. data, Applicant concludes that at a temperature of 1050°C, the average threading dislocation velocity would be 1.4×10^{-3} cm/sec. At temperatures of 1050°C for well-known activation energies for dislocation motion in semiconductor materials, the velocities should be $>>1$ cm/sec.

In accordance with the invention, Applicant supplies data showing a much more modest threading dislocation reduction, and it is supported by the known physical data for dislocation velocities in this semiconductor material. One skilled in the art would be able to follow and understand the purpose and nature of the invention, and achieve a modest but important threading dislocation reduction. Such an invention is useful, for the anneal times are only as long as necessary for the required dislocation flow, and therefore the invention is economically useful.

In view of the foregoing, Applicant contends that the proposed combination of Jewell '864, Bensahel et al. ' 750 and Brasen et al. '205 are not properly combinable, and do not support a *prima facie* case of obviousness under the provisions of 35 USC §103. Accordingly, Applicant submits that claims 1-24 are patentable over the prior art of record.

The application is now considered to be in condition for allowance, and an early indication of same is requested.

Respectfully submitted,

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